PWM BUFFER CIRCUIT FOR ADJUSTING A FREQUENCY AND A DUTY CYCLE OF A PWM SIGNAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a buffer circuit applied with a pulse width modulation (PWM) signal and, more particularly, to a PWM buffer circuit for adjusting a frequency and a duty cycle of a PWM signal.

2. Description of the Related Art

[0002] In recent years, a fan for dissipating heat generally operates with a fan motor whose speed is dominantly controlled through utilizing a PWM signal. Fig. 1 is a circuit block diagram showing a control circuit for speed of a fan motor by using a conventional PWM control method. Referring to Fig. 1, a PWM signal generation unit 10 outputs a PWM signal S1 to a driving circuit 11. Based on the PWM signal S1, the driving circuit 11 outputs a driving signal A to a fan motor 12, thereby controlling the speed of the fan motor 12. More specifically, one of signal characteristics of the PWM signal S1 is known as "duty cycle," i.e., a ratio of a pulse width to a period of the PWM signal S1. Assume that the duty cycle of the PWM signal S1 in Fig. 1 is denoted by a reference numeral D1. In the above-mentioned conventional PWM control method, when the duty cycle D1 of the PWM signal S1 is relatively large, the driving signal A output from the driving circuit 11 causes the fan motor 12 to operate at a relatively high speed. On the other hand, when the duty cycle D1 of the PWM signal S1 is relatively small, the driving signal A output from the driving circuit 11 causes the fan motor 12 to operate at a relatively low speed.

[0003] However, the conventional PWM control method has at least two disadvantages. The

first one of the disadvantages is that the PWM signal S1 to be utilized must have a relatively high frequency, such as 10 kHz or more. When the PWM signal S1 has a frequency lower than 10 kHz, the operation of the fan motor 12 is adversely influenced by switching noise. The second disadvantage is that the duty cycle D1 of the PWM signal S1 to be utilized must be restricted within a range between 30% and 85%, thereby ensuring that the driving circuit 11 and the fan motor 12 can be appropriately controlled by the PWM signal S1.

SUMMARY OF THE INVENTION

[0004] In view of the above-mentioned problems, an object of the present invention is to provide a PWM buffer circuit, arranged in a control circuit for speed of a fan motor, for expanding an applicable range of frequency of a PWM signal to be used as a control signal.

[0005] Another object of the present invention is to provide a PWM buffer circuit, arranged in a control circuit for speed of a fan motor, for expanding an applicable range of duty cycle of a PWM signal to be used as a control signal.

[0006] According to one aspect of the present invention, a PWM buffer circuit includes: a duty cycle converting circuit and a frequency-fixed PWM signal generating circuit. The duty cycle converting circuit receives a first PWM signal and then generates a duty cycle reference voltage based on a first duty cycle of the first PWM signal. The duty cycle reference voltage is a one-to-one mapping function of the first duty cycle. The frequency-fixed PWM signal generating circuit receives the duty cycle reference voltage and then outputs a second PWM signal having a fixed frequency. The second PWM signal has a second duty cycle determined on the basis of the duty cycle reference voltage, and the second duty cycle is a one-to-one mapping function of the duty cycle reference voltage.

[0007] According to another aspect of the present invention, a control circuit for speed of a fan motor includes: a PWM signal generation unit, a PWM buffer circuit, and a driving circuit.

The PWM signal generation unit generates a first PWM signal having a first duty cycle. The PWM buffer circuit is coupled to the PWM signal generation unit for converting the first PWM signal into a second PWM signal having a fixed frequency and a second duty cycle. The driving circuit is coupled to the PWM buffer circuit for outputting a driving signal based on the second PWM signal to the fan motor, thereby controlling the speed of the fan motor.

[0008] In one preferred embodiment of the present invention, the first PWM signal has a frequency higher than 30 Hz and the first duty cycle is located between 5% and 95%. Therefore, the PWM buffer circuit according to the present invention may be arranged in a control circuit for speed of a fan motor so as to expand an applicable range of frequency of the PWM signal as well as an applicable range of duty cycle of the PWM signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The above-mentioned and other objects, features, and advantages of the present invention will become apparent with reference to the following descriptions and accompanying drawings, wherein:

Fig. 1 is a circuit block diagram showing a control circuit for speed of a fan motor by using a conventional PWM control method;

Fig. 2 is a circuit block diagram showing a control circuit for speed of a fan motor arranged with a PWM buffer circuit according to the present invention;

Fig. 3 is a circuit block diagram showing a detailed configuration of a PWM buffer circuit according to the present invention;

Fig. 4(a) is a graph showing that a duty cycle reference voltage V1 is a one-to-one mapping function of a duty cycle D1 of a PWM signal S1;

Fig. 4(b) is a graph showing that a duty cycle D2 of a PWM signal S2 is a one-to-one mapping function of a duty cycle reference voltage V1; and

Fig. 5 is a diagram showing one example of a PWM buffer circuit according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] The preferred embodiments according to the present invention will be described in detail with reference to the drawings.

[0011] Fig. 2 is a circuit block diagram showing a control circuit for speed of a fan motor arranged with a PWM buffer circuit 20 according to the present invention. Referring to Fig. 2, the present invention is different from the prior art shown in Fig. 1 in that a PWM buffer circuit 20 is arranged between the PWM signal generation unit 10 and the driving circuit 11 such that a PWM signal S1 output from the PWM signal generation unit 10 is firstly converted into a PWM signal S2, which is subsequently input into the driving circuit 11. Based on the PWM signal S2, the driving circuit 11 outputs a driving signal B to the fan motor 12.

[0012] More specifically, the PWM buffer circuit 20 converts the PWM signal S1 having the duty cycle D1 and the frequency F1 into the PWM signal S2 having a duty cycle D2 and a frequency F2. In the present invention, the duty cycle D2 and the frequency F2 of the PWM signal S2 are designed to have values that ensure an appropriate control for speed of the fan motor without causing any switching noise. Therefore, with such a configuration, even when the duty cycle D1 and the frequency F1 of the PWM signal S1 do not fall in a range which ensures an appropriate control for speed of the fan motor, an appropriate control for speed of the fan motor is still achieved without causing any switching noise because the driving circuit 11 receives the PWM signal S2, which is the converted signal from the PWM signal S1 by the PWM buffer circuit 20. In other words, the PWM buffer circuit 20 according to the present invention is arranged in the control circuit for speed of the fan motor so as to expand the applicable range of frequency of the PWM signal as well as the applicable

range of duty cycle of the PWM signal.

[0013] As described in the conventional PWM control method shown in Fig. 1, the frequency of the PWM signal S1 must be higher than 10 kHz and the duty cycle D1 thereof must be restrained between 30% and 85%. However, in one embodiment of the present invention, the PWM buffer circuit 20 is designed to convert a PWM signal S1, which has a frequency higher than 30 Hz and a duty cycle located between 5% and 95%, into a PWM signal S2, which has a frequency F2 higher than 10 kHz and a duty cycle D2 located between 30% and 85%. Consequently, the applicable frequency of the PWM signal S1 is expanded to any of values higher than 30 Hz and the applicable duty cycle thereof is expanded to any of values between 5% and 95% through utilizing the PWM buffer circuit 20 according to the present invention.

[0014] Fig. 3 is a circuit block diagram showing a detailed configuration of a PWM buffer circuit 20 according to the present invention. Referring to Fig. 3, the PWM buffer circuit 20 includes a duty cycle converting circuit 21 and a frequency-fixed PWM signal generating circuit 22. More specifically, the duty cycle converting circuit 21 receives the PWM signal S1 and then generates a duty cycle reference voltage V1 based on the duty cycle D1 of the PWM signal S1. In other words, the duty cycle reference voltage V1 is a one-to-one mapping function of the duty cycle D1 of the PWM signal S1, as shown in Fig. 4(a). The frequency-fixed PWM signal generating circuit 22 receives the duty cycle reference voltage V1 and then determines the duty cycle D2 of the PWM signal S2 based on the duty cycle reference voltage V1. In other words, the duty cycle D2 of the PWM signal S2 is a one-to-one mapping function of the duty cycle reference voltage V1, as shown in Fig. 4(b). To sum up, in order to convert the duty cycle D1 into the duty cycle D2, the PWM buffer circuit 20 converts, at a first stage, the duty cycle D1 into the duty cycle reference voltage V1 by utilizing the duty cycle converting circuit 21, followed by converting the duty cycle reference voltage V1 into the duty cycle D2 by utilizing the frequency-fixed PWM signal

generating circuit 22 at a second stage.

[0015] In addition, the frequency-fixed PWM signal generating circuit 22 generates a PWM signal S2 with a fixed frequency regardless of magnitude of the duty cycle reference voltage V1. Accordingly, the frequency-fixed PWM signal generating circuit 22 is designed to output a PWM signal S2 with a frequency F2 that is high enough for avoiding switching noise.

[0016] In one embodiment of the present invention, the frequency-fixed PWM signal generating circuit 22 may be implemented by a microchip control unit, which is set through software programs to perform the desired functions according to the present invention. In another embodiment of the present invention, the frequency-fixed PWM signal generating circuit 22 includes a frequency controller 23 and a PWM signal generator 24, as shown in Fig. 3. More specifically, the frequency controller 23 provides a frequency control signal FC for determining the frequency of the PWM signal S2 generated by the PWM signal generator 24. Based on the duty cycle reference voltage V1 from the duty cycle converting circuit 21 and the frequency control signal FC from the frequency controller 23, the PWM signal generator 24 generates the PWM signal F2 having the duty cycle D2 and the frequency F2.

[0017] Fig. 5 is a diagram showing one example of a PWM buffer circuit 20 according to the present invention. Referring to Fig. 5, the duty cycle converting circuit 21 includes a transistor Q1, a plurality of resistors R1 to R5, a diode Dd1, a capacitor C1, and an operational amplifier OA1. The frequency controller 23 includes a plurality of resistors R6 to R8, a capacitor C2, and an operational OA2. The PWM signal generator 24 includes an operational amplifier OA3 and a resistor R9.

[0018] More specifically, the transistor Q1 has a gate for receiving the PWM signal S1, a drain coupled to a voltage source V_{DD} through the resistor R1, and a source coupled to ground. The diode Dd1 has a P electrode electrically connected to the drain of the transistor Q1 and an N electrode electrically connected to a non-inverting input terminal of the operational

amplifier OA1. The resistor R2 and capacitor C1 are both electrically connected between the N electrode of the diode Dd1 and the ground. The resistor R3 is electrically connected between an inverting input terminal of the operational amplifier OA1 and the ground. The resistor R4 is electrically connected between an output terminal of the operational amplifier OA1 and the ground. The output terminal of the operational amplifier OA1 outputs the duty cycle reference voltage V1 through the resistor R5 to a non-inverting input terminal of the operational amplifier OA3.

[0019] The resistor R6 is electrically connected between an inverting input terminal of the operational amplifier OA2 and the ground. The resistor R7 is electrically connected between the inverting input terminal of the operational amplifier OA2 and an output terminal of the operational amplifier OA2. The capacitor C2 is electrically connected between a non-inverting input terminal of the operational amplifier OA2 and the ground. The resistor R8 is electrically connected between the non-inverting input terminal of the operational amplifier OA2 and the output terminal of the operational amplifier OA2. With such a configuration, the output terminal of the operational amplifier OA2 outputs the frequency control signal FC through the resistor R8 to the inverting input terminal of the operational amplifier OA3. In the example shown in Fig. 5, the frequency control signal FC is a continuous triangular wave signal having a frequency f as expressed in Equation (1):

$$f = \frac{1}{2R_8C_2 \ln\left(1 + 2\frac{R_6}{R_7}\right)} \qquad (1)$$

[0020] In response to the duty cycle reference voltage V1 received at the non-inverting input terminal of the operational amplifier OA3 and the frequency control signal FC received at the inverting input terminal of the operational amplifier OA3, the operational amplifier OA3 outputs the PWM signal S2 from an output terminal through the resistor R9. More specifically, the operational amplifier OA3 works as a voltage comparator such that the operational amplifier OA3 outputs a higher level state of the PWM signal S2 when the duty

cycle reference voltage V1 is larger than the voltage level of the frequency control signal FC whereas the operational amplifier OA3 outputs a lower level state of the PWM signal S2 when the duty cycle reference voltage V1 is smaller than the voltage level of the frequency control signal FC. In such a manner, the PWM signal generator 24 converts the duty cycle reference voltage V1 into the duty cycle D2. In addition, the PWM signal S2 generated by the PWM signal generator 24 has a frequency F2, which is equal to the frequency f of the frequency control signal FC.

[0021] While the invention has been described by way of examples and in terms of preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications.